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10/694,477	10/27/2003	Shunpei Yamazaki	0553-0118.01	4264

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EXAMINER

PRENTY, MARK V

ART UNIT

PAPER NUMBER

2822

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Please find below and/or attached an Office communication concerning this application or proceeding.

CM

Office Action Summary

Application No.

10/694,477

Applicant(s)

YAMAZAKI, SHUNPEI

Examiner

MARK V. PRENTY

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 24,25,28-30,33-35,38,39,41,43,44,46,48,49,51 and 53-59 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 24,25,28-30,33-35,38,39,41,43,44,46,48,49,51 and 53-59 is/are rejected.
- 7) ☒ Claim(s) 54-59 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>June 27, 2005</u> | 6) <input type="checkbox"/> Other: _____ |

This Office Action is in response to the RCE filed on June 27, 2005.

Claims 54-59 are objected to because "the semiconductor layer" lacks antecedent basis (such should apparently read "the semiconductor film"). Correction is required.

Claims 24, 25, 28, 39, 41, 43, 54 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 5,455,791 to Zaleski et al. (Zaleski, already of record) together with United States Patent 6,127,702 to Yamazaki et al. (Yamazaki, already of record).

With respect to independent claim 24, Zaleski discloses a semiconductor device (see the entire patent, including the Fig. 1 disclosure) comprising: a semiconductor film 2b; a pair of first impurity regions 4a, 4b being formed in the semiconductor film; an active region 4c formed between the pair of first impurity regions in the semiconductor film; a floating gate 6 formed over and insulated from the active region; and a control gate 8 formed over and insulated from the floating gate.

The difference between claim 24 and Zaleski is claim 24 further comprises: "at least two second impurity regions formed in said semiconductor film between the pair of first impurity regions; at least one channel region between the at least two second impurity regions, boundaries between the channel region and the at least two second impurity regions extend in a direction along a carrier flow direction of the channel region...wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions."

Yamazaki teaches providing a thin film transistor with at least two such second impurity regions in order to suppress short channel effects, among other things (see the entire patent, including Fig. 1A's impurity regions 104, which connect source and drain regions 101 and 102).

It would have been obvious to one skilled in this art to provide Zaleski's thin film transistor with at least two such second impurity regions that connect source and drain regions 4b and 4a (resulting in a semiconductor device whose floating gate overlaps a boundary between at least one of the source and drain regions (i.e., at least one of the pair of first impurity regions) and the at least two second impurity regions) in order to suppress short channel effects as taught by Yamazaki.

Claim 24 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki.

With respect to dependent claim 25, Yamazaki teaches that its second impurity regions preferably have a striped shape (see column 8, lines 14-21).

Claim 25 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki.

With respect to dependent claim 28, Yamazaki also teaches that thin film semiconductor devices are conventionally used in electronic devices such as a mobile computer, for example (see Yamazaki's Figs. 20-21 disclosure). It would have been further obvious to one skilled in the art to use the obvious Zaleski/Yamazaki semiconductor device in a mobile computer because Yamazaki further teaches that thin

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film semiconductor devices are conventionally used in electronic devices such as a mobile computer.

Claim 28 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki.

With respect to independent claim 39, Zaleski discloses a semiconductor device (see the entire patent, including the Fig. 1 disclosure) comprising: a semiconductor film 2b; a pair of first impurity regions 4a, 4b being formed in the semiconductor film; an active region 4c formed between the pair of first impurity regions in the semiconductor film; a floating gate 6 formed over and insulated from the active region; and a control gate 8 formed over and insulated from the floating gate.

The difference between claim 39 and Zaleski is claim 39 further comprises: "at least two second impurity regions formed in said semiconductor film between the pair of first impurity regions; at least one channel region between the at least two second impurity regions...wherein the at least two second impurity regions have a dot-like shape or an elliptical shape; wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions."

Yamazaki teaches providing a thin film transistor with at least two such second impurity regions in order to suppress short channel effects, among other things (see the entire patent, including Fig. 15A's dot-shaped impurity regions 1401, which extend between source and drain regions 101 and 102).

It would have been obvious to one skilled in this art to provide Zaleski's thin film transistor with at least two such second impurity regions that extend between source and drain regions 4b and 4a (resulting in a semiconductor device whose floating gate overlaps a boundary between at least one of the source and drain regions (i.e., at least one of the pair of first impurity regions) and the at least two second impurity regions) in order to suppress short channel effects as taught by Yamazaki.

Claim 39 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki.

With respect to dependent claim 41, Zaleski's semiconductor device further comprises a substrate 2a/3, wherein the semiconductor film 2b is formed over the substrate.

Claim 41 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki.

With respect to dependent claim 43, Yamazaki also teaches that thin film semiconductor devices are conventionally used in electronic devices such as a mobile computer, for example (see Yamazaki's Figs. 20-21 disclosure). It would have been further obvious to one skilled in the art to use the obvious Zaleski/Yamazaki semiconductor device in a mobile computer because Yamazaki further teaches that thin film semiconductor devices are conventionally used in electronic devices such as a mobile computer.

Claim 43 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki.

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With respect to dependent claims 54 and 57, Zaleski's device further comprises an insulating layer 3 that underlies semiconductor film 2b, and Yamazaki further teaches that such an insulating layer should comprise the same conductivity type impurity element as the at least two second impurity regions (see the Embodiment 11 disclosure at columns 28-29).

Claims 54 and 57 are thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki.

Claims 29, 30, 33, 34, 35, 38, 44, 46, 48, 49, 51, 53, 55, 56, 58 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 5,455,791 to Zaleski et al. (Zaleski, already of record) together with United States Patent 6,127,702 to Yamazaki et al. (Yamazaki, already of record) and United States Patent 5,814,854 to Liu et al (Liu, already of record).

Independent claim 29 parallels independent claim 24 except that claim 29 further recites a NOR type circuit comprising a plurality of transistors. The explanation of the above rejection of claim 24 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki is thus hereby incorporated by reference into this rejection of claim 29 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

The difference, therefore, between independent claim 29 and the obvious Zaleski/Yamazaki device is claim 29 recites a NOR type circuit.

Liu, however, teaches that EEPROM devices are conventionally used to form NOR type circuits (see column 4, lines 1-16).

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It would have been further obvious to one skilled in the art use the obvious Zaleski/Yamazaki EEPROM device in a NOR type circuit because Liu teaches that EEPROM devices are conventionally used to form a NOR type circuit.

Claim 29 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

Independent claim 29's dependent claims 30 and 33 parallel independent claim 24's dependent claims 25 and 28 (addressed above) and are thus also rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

Independent claim 34 parallels independent claim 24 except that claim 34 further recites a NAND type circuit comprising a plurality of transistors. The explanation of the above rejection of claim 24 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki is thus hereby incorporated by reference into this rejection of claim 34 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

The difference, therefore, between independent claim 34 and the obvious Zaleski/Yamazaki device is claim 29 recites a NAND type circuit.

Liu, however, teaches that EEPROM devices are conventionally used to form NAND type circuits (see column 4, lines 1-16).

It would have been further obvious to one skilled in the art use the obvious Zaleski/Yamazaki EEPROM device in a NAND type circuit because Liu teaches that EEPROM devices are conventionally used to form a NAND type circuit.

Claim 34 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

Independent claim 34's dependent claims 35 and 38 parallel independent claim 24's dependent claims 25 and 28 (addressed above) and are thus also rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

Independent claim 44 parallels independent claim 39 except that claim 44 further recites a NOR type circuit comprising a plurality of transistors. The explanation of the above rejection of claim 39 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki is thus hereby incorporated by reference into this rejection of claim 44 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

The difference, therefore, between independent claim 44 and the obvious Zaleski/Yamazaki device is claim 44 recites a NOR type circuit.

Liu, however, teaches that EEPROM devices are conventionally used to form NOR type circuits (see column 4, lines 1-16).

It would have been further obvious to one skilled in the art use the obvious Zaleski/Yamazaki EEPROM device in a NOR type circuit because Liu teaches that EEPROM devices are conventionally used to form a NOR type circuit.

Claim 44 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

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Independent claim 44's dependent claims 46 and 48 parallel independent claim 39's dependent claims 41 and 43 (addressed above) and are thus also rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

Independent claim 49 parallels independent claim 39 except that claim 49 further recites a NAND type circuit comprising a plurality of transistors. The explanation of the above rejection of claim 39 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki is thus hereby incorporated by reference into this rejection of claim 49 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

The difference, therefore, between independent claim 34 and the obvious Zaleski/Yamazaki device is claim 49 recites a NAND type circuit.

Liu, however, teaches that EEPROM devices are conventionally used to form NAND type circuits (see column 4, lines 1-16).

It would have been further obvious to one skilled in the art use the obvious Zaleski/Yamazaki EEPROM device in a NAND type circuit because Liu teaches that EEPROM devices are conventionally used to form a NAND type circuit.

Claim 49 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

Independent claim 49's dependent claims 51 and 53 parallel independent claim 39's dependent claims 41 and 43 (addressed above) and are thus also rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.


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With respect to dependent claims 55, 56, 58 and 59, Zaleski's device further comprises an insulating layer 3 that underlies semiconductor film 2b, and Yamazaki further teaches that such an insulating layer should comprise the same conductivity type impurity element as the at least two second impurity regions (see the Embodiment 11 disclosure at columns 28-29).

Claims 55, 56, 58 and 59 are thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

The applicant's argument in the paragraph bridging pages 12 and 13 of its response is not persuasive because it merely argues the Zaleski and Yamazaki references separately instead of addressing the 35 U.S.C. 103(a) rejection's explanation of how those references are combined and result in the claimed invention. The applicant cannot show nonobviousness by attacking references individually where the rejection is based on a combination of references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.


Mark V. Prenty
Primary Examiner